REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

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Original date of drawing
YY MM DD
12-11-20

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TITLE

MICROCIRCUIT, DIGITAL-LINEAR, CMOS 1.8 V TO 5.5 V, 2.5 Ω, 2:1 MUX/SPDT SWITCH, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/12650

REV

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AMSC N/A

5962-V028-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS 1.8 V to 5.5 V, 2.5 Ω, 2:1 Mux/SPDT switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12650	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG719-EP	CMOS 1.8 V to 5.5 V, 2.5 Ω, 2:1 Mux/SPDT switch

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	6	JEDEC MO-178-AB	Small Outline Transistor Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.3 V to +7.0 V
Analog, Digital inputs	-0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 2/
Peak current, S or D	100 mA (Pulsed at 1 ms, 10% duty cycle max)
Continuous current, S or D	30 mA
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
Case outline X, θ_{JA} Thermal impedance	186.45 °C/W 3/
Lead soldering:	
Reflow, Peak temperature	260(+0/-5) °C
Time at peak temperature	20 sec to 40 sec
ESD	1 kV

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Over voltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.
3/ Measured on a 4-layer board.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 On resistance. The On resistance shall be as shown in figure 6.

3.5.7 Off leakage. The Off leakage shall be as shown in figure 7.

3.5.8 On leakage. The On leakage shall be as shown in figure 8.

3.5.9 Switching times. The switching times shall be as shown in figure 9.

3.5.10 Break before make time delay, t_D. The break before make time delay, t_D shall be as shown in figure 10.

3.5.11 Off isolation. The Off isolation shall be as shown in figure 11.

3.5.12 Channel to Channel crosstalk. The Channel to Channel crosstalk shall be as shown in figure 12.

3.5.13 Bandwidth. The Bandwidth shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions V_{DD} = 5 V ±10%, GND = 0 V unless otherwise noted	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to V_{DD}, I_S = -10 mA		2.5					Ω
		See FIGURE 6			4			7	
On resistance match between channels	Δ R_{ON}	V_S = 0 V to V_{DD}, I_S = -10 mA		0.1				0.4	Ω
On resistance Flatness	$R_{FLAT(ON)}$	V_S = 0 V to V_{DD}, I_S = -10 mA		0.75				1.5	Ω
Leakage current I_S (Off) (V_{DD} = 5.5 V)									
Source off leakage	I_S (Off)	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V; See FIGURE 7		±0.01	±0.25			1	nA
Channel On leakage	I_D, $I_{S\,(ON)}$	V_S = V_D = 1 V or V_S = V_D = 4.5 V See FIGURE 8		±0.01	±0.25			5	nA
Digital inputs									
Input high voltage	V_{IH}					2.4			V
Input low voltage	V_{IL}							0.8	
Input current	I_{NL} or I_{NH}	V_{IN} = V_{INL} or V_{INH}		0.005				±0.1	µA
Dynamic characteristics 2/									
	t_{ON}	R_L = 300 Ω, C_L 35 pF,		7				12	ns
	t_{OFF}	V_S = 3 V, See FIGURE 9		3				6	
Break before Make time delay	t_D	R_L = 300 Ω, C_L 35 pF, V_{S1} = V_{S2} = 3 V, See FIGURE 10		8		1			
Off Isolation		R_L = 50 Ω, C_L 5 pF, f = 10 MHz, See FIGURE 11		-67					dB
		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 11		-87					
Channel to channel crosstalk		R_L = 50 Ω, C_L 5 pF, f = 10 MHz, See FIGURE 12		-62					
		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 12		-82					
Bandwith -3 dB		R_L = 50 Ω, C_L 5 pF, See FIGURE 13		200					MHz
C_S (Off)				7					pF
C_D, C_S (ON)				27					
Power requirements (V_{DD} = 5.5 V, Digital inputs = 0 V or 5,5 V)									
	I_{DD}			0.001				1.0	µA

See footnote at end of table.

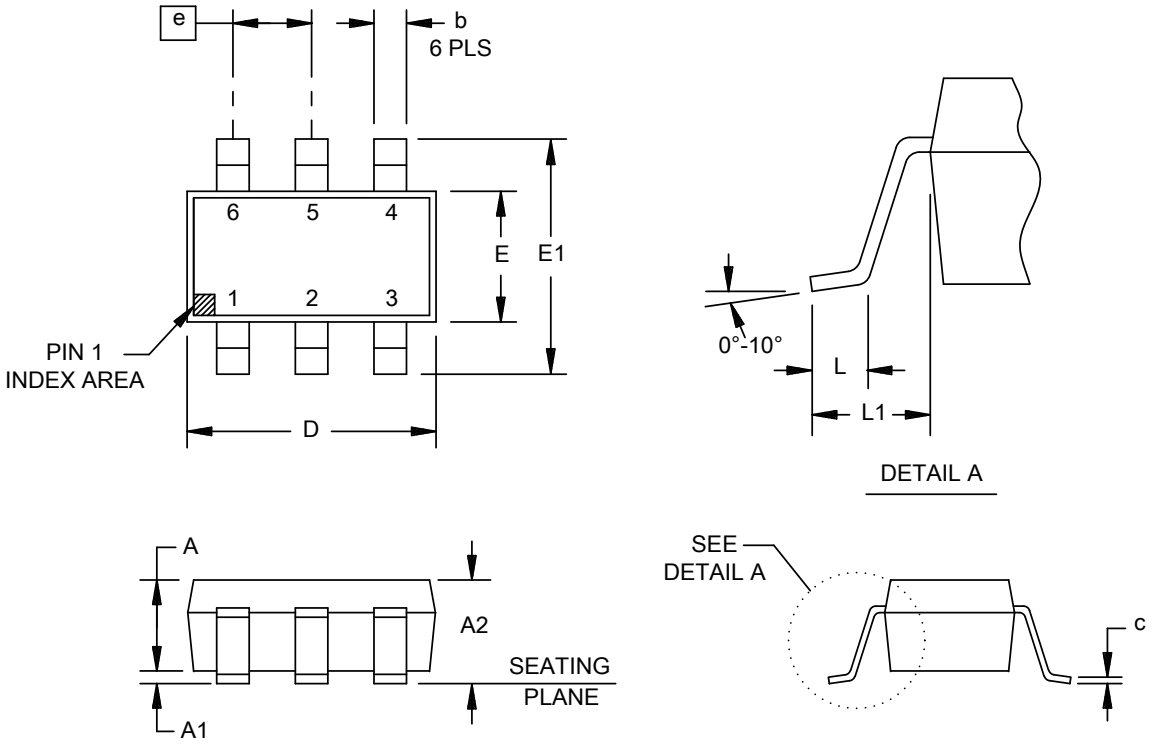
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions V_{DD} = 3 V ±10%, GND = 0 V unless otherwise noted	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to V_{DD}, I_S = -10 mA		6					Ω
		See FIGURE 6						12	
On resistance match between channels	Δ R_{ON}	V_S = 0 V to V_{DD}, I_S = -10 mA		0.1				0.4	Ω
On resistance Flatness	$R_{FLAT(ON)}$	V_S = 0 V to V_{DD}, I_S = -10 mA					2.5		Ω
Leakage current I_S (Off) (V_{DD} = 3.3 V)									
Source off leakage	I_S (Off)	V_S = 3 V/1 V, V_D = 1 V/3 V; See FIGURE 7		±0.01	±0.25			1	nA
Channel On leakage	I_D, $I_{S (ON)}$	V_S = V_D = 1 V or VS = VD = 3 V See FIGURE 8		±0.01	±0.25			5	nA
Digital inputs									
Input high voltage	V_{IH}					2.0			V
Input low voltage	V_{IL}							0.8	
Input current	I_{NL} or I_{NH}	V_{IN} = V_{INL} or V_{INH}		0.005				±0.1	µA
Dynamic characteristics 2/									
	t_{ON}	R_L = 300 Ω, C_L 35 pF,		10				15	ns
	t_{OFF}	V_S = 2 V, See FIGURE 9		4				8	
Break before Make time delay	t_D	R_L = 300 Ω, C_L 35 pF, V_{S1} = V_{S2} = 2 V, See FIGURE 10		8		1			
Off Isolation		R_L = 50 Ω, C_L 5 pF, f = 10 MHz, See FIGURE 11		-67					dB
		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 11		-87					
Channel to channel crosstalk		R_L = 50 Ω, C_L 5 pF, f = 10 MHz, See FIGURE 12		-62					
		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 12		-82					
Bandwith -3 dB		R_L = 50 Ω, C_L 5 pF, See FIGURE 13		200					MHz
C_S (Off)				7					pF
C_D, C_S (ON)				27					
Power requirements (V_{DD} = 5.5 V, Digital inputs = 0 V or 5,5 V)									
	I_{DD}			0.001	1.0				µA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Guaranteed by design, not subject to production test.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.90	1.30	E	1.50	1.70
A1	0.05	0.15	E1	2.60	3.00
A2	0.95	1.45	e	0.95 BSC	
b	0.30	0.50	L	0.35	0.55
D	2.80	3.00	L1	0.60 BSC	

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-15-AB3.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IN	6	S2
2	V_{DD}	5	D
3	GND	4	S1

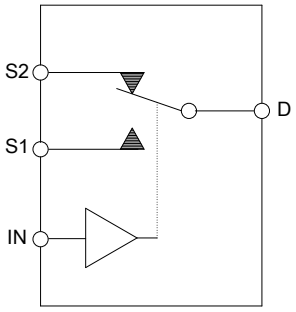
FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
Number	Mnemonic	
1	IN	Digital switch control pin.
2	V_{DD}	Most positive power supply pin.
3	GND	Ground (0 V) reference pin.
4	S1	Source terminal. Can be used as an input or output
5	D	Drain terminal. Can be used as an input or output
6	S2	Source terminal. Can be used as an input or output

FIGURE 3. Terminal function.

Input IN	Switch S1	Switch S2
0	On	Off
1	Off	On

FIGURE 4. Truth table



NOTES:
1. Switches shown for a logic 1 input.

FIGURE 5. Functional block diagram.

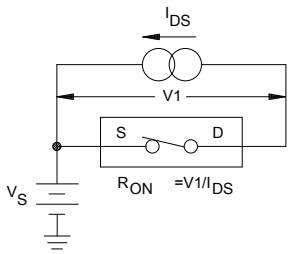


FIGURE 6. On resistance.

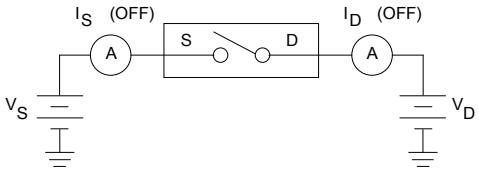


FIGURE 7. Off leakage.

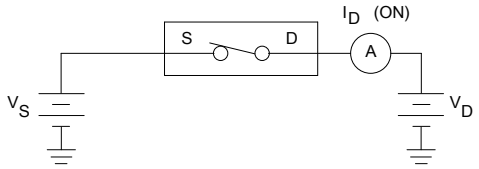


FIGURE 8. On leakage.

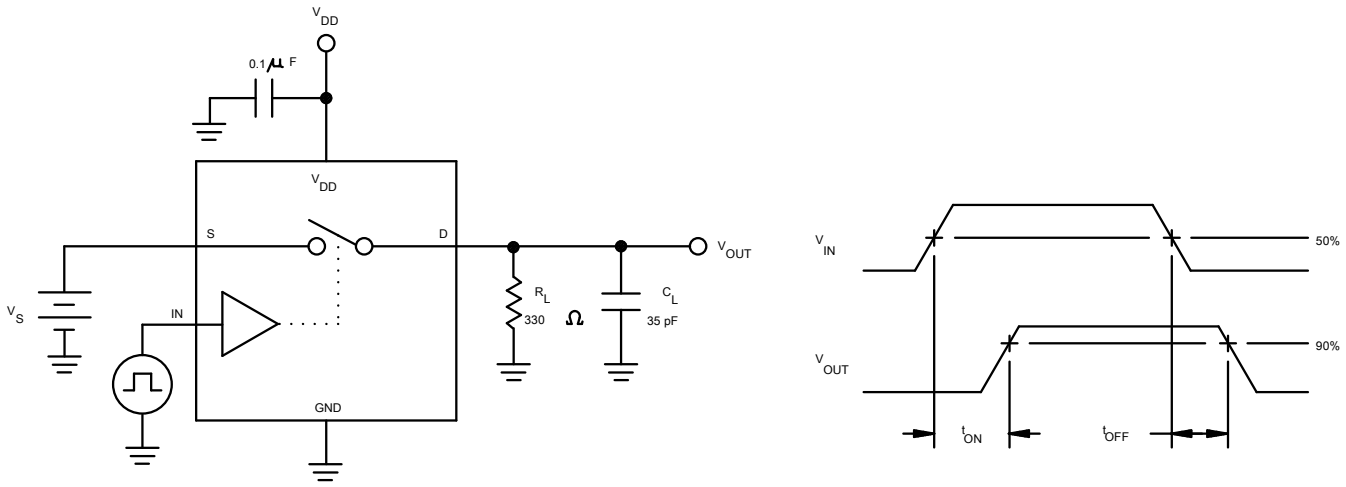


FIGURE 9. Switching times.

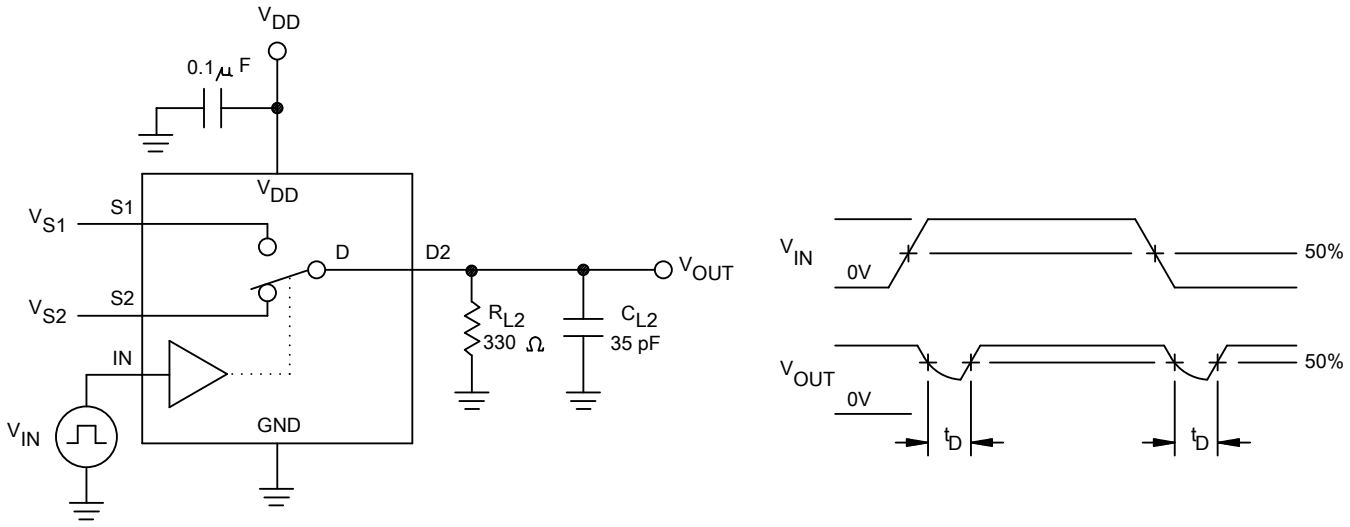


FIGURE 10. Break before make time delay, t_D.

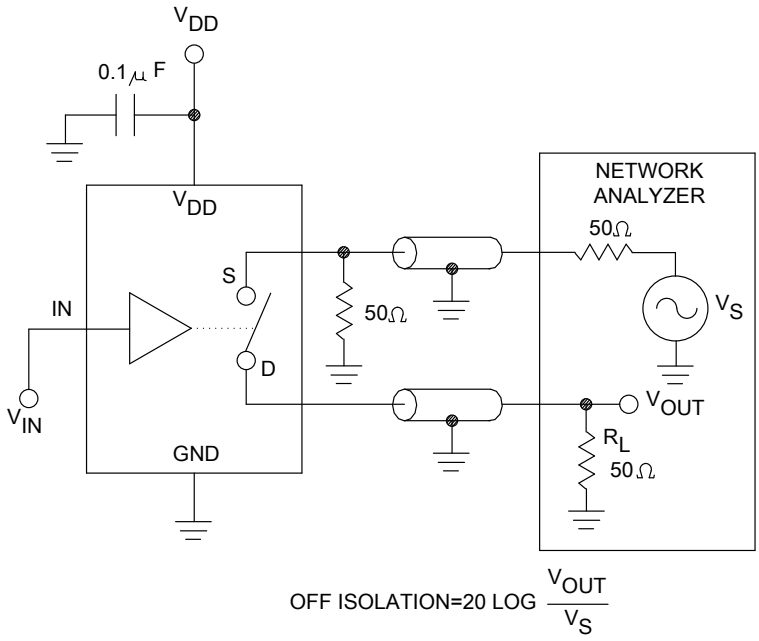


FIGURE 11. Off isolation.

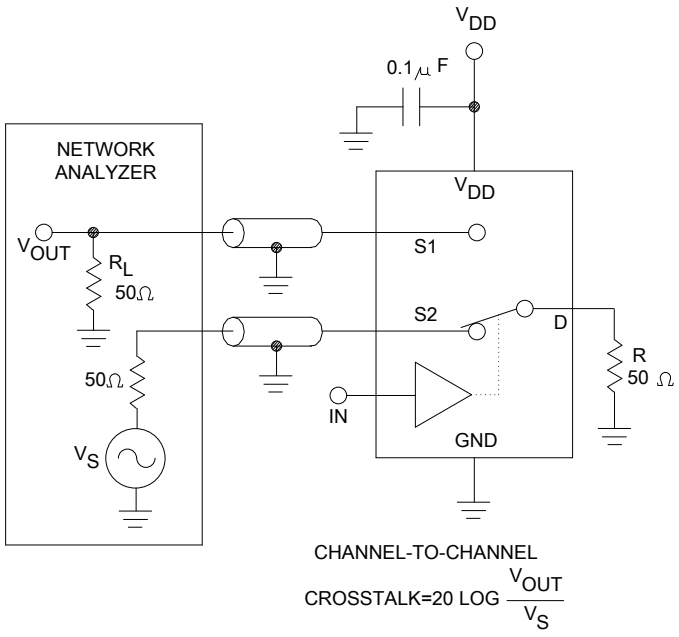


FIGURE 12. Channel to Channel crosstalk.

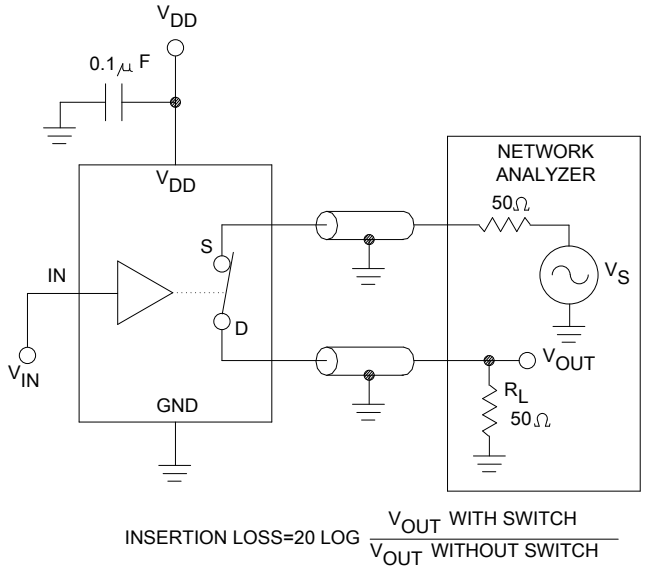


FIGURE 13. Bandwidth.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12650-01XE	24355	ADG719SRJZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106